AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (Previously Presented) A method of manufacturing a capacitor in semiconductor devices, the method comprising:

forming a silicon oxide film on a surface of a silicon substrate;

forming a nitride film on said silicon oxide film;

forming a contact hole by sequentially etching a portion of said nitride film and said silicon oxide film;

depositing a doped polysilicon layer over the entire surface of said silicon substrate, said doped polysilicon layer filling said contact hole;

performing an etch-back process to remove a portion of said doped polysilicon layer, said etch-back process leaving said doped polysilicon layer in said contact hole;

forming an ohmic contact layer over said doped polysilicon layer in said contact hole;

forming an anti-diffusion film on said ohmic contact layer;

forming a silicate glass film over the entire surface of said silicon substrate including said anti-diffusion film;

forming a concave hole by etching a portion of said silicate glass film, said concave hole having an internal wall;

forming a Ruthenium lower electrode on said internal wall of said concave hole;

performing a NH_3-plasma process and a N_2O-plasma process sequentially on said Ruthenium lower electrode;

forming a BST dielectric film on said Ruthenium lower electrode which had undergone said NH_3-plasma process and said N_2O-plasma process;

crystallizing said BST dielectric film, said crystallizing including performing a rapid thermal process;

forming an upper electrode on said BST dielectric film, said BST dielectric film, said lower Ruthenium electrode and said upper electrode forming said capacitor; and

performing a thermal treatment to stabilize said capacitor.

2. (Original) The method according to claim 1, wherein said nitride film comprises a thickness of about 300~1000 Å.

3. (Original) The method according to claim 1, wherein said depositing said doped polysilicon layer comprises chemical vapor deposition and said doped polysilicon layer comprises a thickness of about 700~3000 Å.

4. (Original) The method according to claim 1, wherein said

performing said etch-back process etches said doped polysilicon layer to a depth of about 200~1500 Å into said contact hole.

5. (Original) The method according to claim 1, wherein said forming said ohmic contact layer comprises depositing at least one of Titanium and Cobalt having a thickness of about 100~500 Å over the entire surface of said silicon substrate, including said doped polysilicon layer remaining within said contact hole, performing a thermal process to form titanium silicide and cobalt silicide on said doped polysilicon layer remaining within said contact hole, and then removing the remaining at least one of Titanium and Cobalt.

6. (Original) The method according to claim 1, wherein said forming said anti-diffusion film comprises depositing at least one of TiN and TiAlN having a thickness of about 700~3000 Å over the entire surface of said silicon substrate, and then removing the at least one of said TiN and the TiAlN except from said contact hole, the depositing at least one of TiN and TiAlN including at least one of a physical vapor deposition method and a chemical vapor deposition method, and the removing at least one of TiN and TiAlN including a chemical mechanical polishing method.

7. (Original) The method according to claim 1, wherein said

forming said silicate glass film comprises depositing at least one of USG and PSG having a thickness of about 2000~15000 Å.

8. (Previously Presented) The method according to claim 1, wherein said forming said Ruthenium lower electrode comprises depositing Ruthenium having a thickness of about 100~500 Å over the entire surface of said silicon substrate, and then removing the Ruthenium, except from said internal wall of said concave hole, said depositing Ruthenium including at least one of a sputtering method and a chemical vapor deposition method, and said removing the Ruthenium including at least one of a chemical mechanical polishing method and an etch-back process.

9. (Original) The method according to claim 1, wherein said performing said NH_3-plasma process comprises a set of conditions including power that is about 100~500 W, pressure that is about 0.5~2.0 Torr, flow rate of NH_3 that is about 200~2000 sccm, and temperature that is about 350~700°C.

10. (Original) The method according to claim 1, wherein said performing said N_2O-plasma process comprises a set of conditions including power that is about 100~500 W, pressure that is about 0.5~2.0 Torr, flow rate of N_2O that is about 200~2000 sccm, and temperature that is about 350~700°C.

11. (Original) The method according to claim 1, wherein said depositing said BST dielectric film comprises a chemical vapor deposition method and said BST dielectric film comprises a thickness of about 150~500 Å.

12. (Original) The method according to claim 1, wherein said performing said rapid thermal process comprises at least one of a mixture gas of oxygen and nitrogen and a mixture gas of oxygen and argon at a temperature of about 500~750°C for about 10~180 seconds.

13. (Canceled)

14. (Previously Presented) The method according to claim 1, wherein said forming said upper electrode comprises depositing at least one of Ruthenium, Iridium, and Platinum having a thickness of about 150~500 Å, the depositing at least one of Ruthenium, Iridium, and Platinum including at least one of a sputtering method and a chemical vapor deposition method.

15. (Original) The method according to claim 1, wherein said performing said thermal treatment comprises at least one of a mixture gas of oxygen and nitrogen and a mixture gas of oxygen and argon at a temperature of about 400~800°C for about 1~130 minutes.

16. (Original) The method according to claim 1, wherein the silicon oxide film comprises an interlayer insulating layer.

17. (Canceled)

18. (Canceled)

19. (Canceled)

20. (Canceled)